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Allegro PCB Design Solution. October 18, 2018 Cadence PCB Solutions. Systems companies are impacted by new devices and design methodologies offered by the semiconductor industry. New devices often bring more challenges, like

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increasing pin counts packaged in shrinking pin pitch ball grid arrays (BGAs). Additionally, new devices use evolving standards-based interfaces, such as DDR3, DDR4, PCI Express® (PCIe®) Gen3, USB 3.0, and others, that may require learning new ways to implement them on ...

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Tabbed Routing - The Next Generation High Speed Routing Solution (Reason 7

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of 10) Improve Route Channel Utilization with Tabbed Routing Tabbed routing is a new method in which trapezoidal shapes called tabs are added to parallel traces to control impedance in the pin field/breakout regions, and reduce crosstalk in open field regions.

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Community

Page 2 FEATURES PCB EDITOR TECHNOLOGY CONSTRAINT-DRIVEN PCB EDITING ENVIRONMENT At the heart of Cadence PCB design solutions is a PCB editor—an intuitive, easy-to-use, constraint-driven environment for creating and editing simple to complex PCBs.

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Select the DRC, right-click, and choose Display. The Allegro layout editor automatically navigates to the DRC location and the design rule marker indicates the violation. To learn in detail about this feature, watch the How to Run

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a RAVEL Rule from the GUI video on the Cadence Support portal.

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MUNICH, Germany, May 3, 2016 —Today at CDNLive EMEA, Cadence Design Systems, Inc. (NASDAQ: CDNS) announced new capabilities for OrCAD®

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Capture, PSpice® Designer and PCB Designer 17.2-2016 that address challenges with flex and rigid-flex design as well as mixed-signal simulation complexities in IoT, wearables and wireless mobile devices.

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